IN THE SPECIFICATION

The paragraph beginning on page 8, line 7 is sought to be rewritten as follows:

As noted above, virtual memory architectures have long been used in general-purpose computers. However, there **[[turn]]** **turns** out to be some surprising difficulties in using this idea in computer graphics (especially for texture memory). The present application discloses several innovations related to virtualization and caching of texture memory.

The paragraph beginning on page 8, line 31 is sought to be rewritten as follows:

Notable (and separately innovative) features of the virtual texture mapping architecture described in the present application include at least the following: A single chip solution is provided; Two or three levels of texture memory hierarchy are supported; The page faulting is all done in hardware with no host intervention; The texture memory management function can be used to manage texture storage in the host memory in addition to the texture storage in our normal texture memory; multiple memory pools are supported; and multiple rasterizers can be supported. The present application is one of nine applications filed simultaneously, which are all contemplated to be implemented together in a common system. The other applications are attorney's docket numbers TD-151 through TD-159 **(U.S. non-provisional applications 09/591,533, 09/591,532, 09/591,228, 09/591,231, 09/591,225, 09/591,226, 09/591,229, 09/591,230, and 09/591,227 all filed 6/9/2000)**, and all are hereby incorporated by reference.

The paragraph beginning on page 11, line 5 is sought to be rewritten as ~~follows:~~

The following pages give details of a sample embodiment of the preferred rendering accelerator chip (referred to as 'P3" in the following document, although not all details may apply to every chip revision marketed as P3). Particular attention will be paid to the Texture Read Unit of this chip, where many of the disclosed inventions are implemented. Commonly-owned US applications 09/322,828, 09/280,250, and 09/266,052 provide various other details of the contexts within which the claimed inventions are most preferably implemented, and are all incorporated herein by reference. The present application is one of nine applications filed simultaneously, which are all contemplated to be implemented together in a common system. The other applications are attorney's docket numbers TD-151 through TD-159 **(U.S. non-provisional applications 09/591,533, 09/591,532, 09/591,228, 09/591,231, 09/591,225, 09/591,226, 09/591,229, 09/591,230, and 09/591,227 all filed 6/9/2000)**, and all are hereby incorporated by reference. Also incorporated by reference are commonly owned co-pending U.S. provisional priority applications 60/138,350 and 60/138,248, both filed **June 9, 1999**, and provisional applications 60/143,826, 60/143,712, 60/143,661, 60/143,655, 60/143,822, 60/143,825, 60/143,654, 60/143,660, 60/143,650, all filed on July 13, 1999.